# H. Umut Suluhan

suluhan@arizona.edu • linkedin • github •

## EDUCATION

**Electrical and Computer Engineering** *PhD* — Expected May 2027
University of Arizona, Tucson, AZ — GPA: 3.75/4.0
**Computer Science** *BS* — February 2023
Ozyegin University, Istanbul, Turkey — GPA: 3.72/4.0

## WORK EXPERIENCE

**University of Arizona** | *Graduate Research Assistant* — Jan 2023 - Present
**Scientific and Technological Research Council of Türkiye** | *Undergraduate Research Assistant* — Sep 2021 - Dec 2022

## RESEARCH FOCUS

**Runtime System Design and Placement Algorithms for Coarse-Scale Programmable Heterogeneous SoCs**

- Productive architecture exploration along with application development and deployment for seamless dynamic workload execution on a wide range of heterogeneous SoCs
- Design and development of a reinforcement learning environment targeting placement of heterogeneous kernels on a coarse-grained 2D systolic array architectures, in which users can integrate and evaluate new placement heuristics

## RELEVANT PROJECTS

**Deployment of PyTorch Models on Heterogeneous SoCs**

- Designed and developed a framework that transforms PyTorch models into C++ representation to be able to deploy on systems composed of a pool of accelerators and CPU cores
- Demonstrated ability to execute range of machine learning models concurrently on a single heterogeneous system composed of Convolution, FFT accelerators and ARM CPU Cores emulated on the Xilinx ZCU102 platform

**RISC-V Based Heterogeneous SoC Design**

- Built an FPGA image comprising heterogeneous set of RISC-V cores and FFT accelerators including their peripherals, DMA engine, and interconnect along with a bootable Linux
- Design space exploration based on FPGA emulation of heterogeneous SoC on Xilinx Virtex 7 VC707
- Deployed signal processing applications with dynamic workload scenarios and exposed the trade-off between scheduler complexity, degree of heterogeneity, and workload complexity

## PUBLICATIONS

- H. U. Suluhan, S. Gener, A. Fusco, J. Mack, I. Dagli, M. Belviranli, C. Edemen, and A. Akoglu, "A Runtime Manager Integrated Emulation Environment for Heterogeneous SoC Design with RISC-V Cores," in Proc. 2024 IEEE Int. Parallel Distrib. Process. Symp. Workshops (IPDPSW), 2024, pp. 23-30.
- H. U. Suluhan, S. Gener, A. Fusco, H. F. Ugurdag and A. Akoglu, "PyTorch and CEDR: Enabling Deployment of Machine Learning Models on Heterogeneous Computing Systems" 2023 20th ACS/IEEE International Conference on Computer Systems and Applications (AICCSA), Giza, Egypt, 2023, pp. 1-8.
- J. Mack, S. Gener, S. Hassan, H. U. Suluhan, and A. Akoglu, *"CEDR-API: Productive, performant programming of domain-specific embedded systems"* in 2023 IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW), 2023, pp. 16 25.
- H. U. Suluhan, H. F. Ates, and B. K. Gunturk, *"Dual camera based high spatio-temporal resolution video generation for wide area surveillance"* in 2022 18th IEEE International Conference on Advanced Video and Signal Based Surveillance (AVSS). IEEE, 2022, pp. 1–8.

## FUNDED PROJECTS

- DARPA-DSSoC: Domain-Focused Advanced Software-Reconfigurable Heterogeneous System on Chip (DASH-SoC) Grant # FA8650-18-2-7860
- DARPA-PROWESS : Dynamic Runtime Domain-Focused Software-Reconfigurable Heterogeneous (DR-DASH) Processor HR001123C0130

## SKILLS

- **Programming Languages:** C, C++, Python, Verilog, CUDA, Java
- **Hardware and Embedded Design:** Heterogeneous SoC, RTL Design, Rocket Chip Generator, FPGA Design Tools, FPGA Emulation, ASIC Design Flow, CPU-GPU architecture
- **Software Experience:** PyTorch, Synopsys VCS, MPI, OpenMP, Vivado, Linux, Git

## COURSE WORK

- High-Performance Computing: Technology, Architecture, and Algorithms, Computer Architecture and Design, Fundamentals of Computer Networks, Cyber Security - Concept, Theory, Practice