Y. Serhan Gener

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Objective

Seeking an internship opportunity to leverage my hands-on hardware and software expertise in FPGA-based design and development, runtime resource management frameworks, and programming languages to contribute to cutting-edge hardware design for real-world applications. Aiming to gain practical experience, drive impactful results, and broaden my knowledge in the field of hardware innovation.

Experience

University of Arizona – Department of Electrical and Computer Engineering **Tucon, AZ, USA**
Graduate Research Assistant, Reconfigurable Computing Lab, Advisor: Prof. Ali Akoglu *2022 – Present*

- Design and development of novel value-based resource management heuristics for heterogeneous SoCs as part of the project funded by DARPA DSSOC, SpaceBACN, and PROWESS Programs
- FPGA-based emulation of full scale heterogeneous SoC on the Synopsys HAPS-100 multi-FPGA platform
- Design and development of a runtime framework for deploying GNURadio workflows on heterogeneous SoCs

Pi-Radio **Remote**
Internship *June 2021 – September 2021*

- Implementation of communication components of the SDR on Xilinx RFSoC

University of California - Riverside – Computer Science **Riverside, CA, USA**
Teaching Assistant *2019 – 2022*

- Lab management and instruction for embedded systems curriculum covering Introduction to Embedded Systems and Intermediate Embedded and Real-Time Systems

Graduate Research Assistant, Advisor: Prof. Philip Brisk *2018 – 2022*

- RTL-based design of vector processor based Fully Homomorphic Encryption on FPGA

Yeditepe University – Computer Science and Engineering **Istanbul, Turkey**
Graduate Research Assistant, Advisor: Prof. Sezer Goren *2015 – 2018*

- Design of Z3-based SMT solver for a secure processor architecture
- A memory efficient RTL design for continuous functions on Xilinx Artix-7 FPGA platform
- RTL-based area and timing oriented dynamic optimization of Binary Tree Constant Division

Teaching Assistant *2015 – 2018*

- Lab management for core freshman to senior level CS courses covering Computer Engineering Concepts and Algorithms, Fundamentals of Computer Programming, Systems Programming and Assembly Language, File Organization, Algorithms and Programming, Embedded Systems Programming, Introduction to Digital Systems, Software Development Methodologies, and Concurrent Programming

Technical Skills

Programming Languages: Verilog, Scala/Chisel, Python, MATLAB, Perl, Bash, AWK, Java, CUDA, C/C++
Tools: Xilinx Vitis and Vivado, Jupyter Notebook, Eclipse ISE, Unity IDE, Google Colab
Familiar with: HLS design, Petalinux, Tensorflow, Z3 SMT Solver

Select Publications

Gener, Serhan, Sahil Hassan, and Ali Akoglu. "Value-Based Resource Management at SoC Scale." *Proceedings of the SC'23 Workshops of The International Conference on High Performance Computing, Network, Storage, and Analysis.* 2023. doi:10.1145/3624062.3624243

Serhan, Gener, Dattilo Parker, Gajaria Dhruv, Fusco Alexander, and Akoglu Ali. "Gpu-based and streaming-enabled implementation of pre-processing flow towards enhancing optical character recognition accuracy and efficiency." *Cluster Computing, 26, 3407–3419* 2023. doi:10.1007/s10586-023-04137-0

Joshua Mack, **Serhan Gener**, Sahil Hassan, H. Umut Suluhan, and Ali Akoglu, "CEDR-API: Productive, Performant Programming of Domain-Specific Embedded Systems." *IEEE International Parallel and Distributed Processing Symposium Workshops (IPDPSW)*, pp. 16-25. 2023. doi:10.1109/IPDPSW59300.2023.00016

Gener, Serhan, Parker Newton, Daniel Tan, Silas Richelson, Guy Lemieux, and Philip Brisk. "An fpga-based programmable vector engine for fast fully homomorphic encryption over the torus." *In SPSL: Secure and Private Systems for Machine Learning (ISCA Workshop)*. 2021.

Gener, Y. Serhan, Furkan Aydin, Sezer Gören, and H. Fatih Ugurdag. "Semi-and fully-random access LUTs for smooth functions." *In VLSI-SoC: New Technology Enabler: 27th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2019, Cusco, Peru, October 6–9, 2019, Revised and Extended Selected Papers 27*, pp. 279-306. Springer International Publishing, 2020. doi:10.1007/978-3-030-53273-4_13

Ugurdag, H. Fatih, Florent De Dinechin, **Y. Serhan Gener**, Sezer Gören, and Laurent-Stéphane Didier. "Hardware division by small integer constants." *IEEE Transactions on Computers* 66, no. 12 (2017): 2097-2110. doi:10.1109/TC.2017.2707488

Education

University of Arizona, AZ, USA **2022 – Present**
Ph.D. in Electrical and Computer Engineering *GPA: 3.8/4*
Advisor: Prof. Ali Akoglu

University of California - Riverside, CA, USA **2018 – 2022**
Ph.D. in Computer Science - Transfer to UofA *GPA: 3.91/4*
Advisor: Prof. Philip Brisk

Yeditepe University, Istanbul, Turkey **2017 – 2018**
Ph.D. in Computer Science and Engineering - Transfer to UCR
Advisor: Prof. Sezer Goren

Yeditepe University, Istanbul, Turkey **2015 – 2017**
M.Sc. in Computer Science and Engineering *GPA: 4.0/4.0*
Advisor: Prof. Sezer Goren
Co-advisor: Prof. Fatih Ugurdag

Yeditepe University, Istanbul, Turkey **2011 – 2015**
B.Sc. in Computer Science and Engineering *GPA: 3.72/4.0*
Advisor: Prof. Sezer Goren

Involved Projects

DARPA-DSSoC: Domain-Focused Advanced Software-Reconfigurable Heterogeneous System on Chip (DASH-SoC) Grant # FA8650-18-2-7860

DARPA-PROWESS: Dynamic Runtime Domain-Focused Software-Reconfigurable Heterogeneous (DR-DASH) Processor #HR001123C0130

DARPA-SPACEBACN: Configurable Optical Communications via Heterogeneous-Processing Optimized Node (COCHON) Grant #HR00112290043

National Science Foundation (NSF): I/UCRC Cloud and Autonomic Computing Grant # NSF CNS-1624668