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EDUCATION

UNIVERSITY OF ARIZONA, COLLEGE OF ENGINEERING GRADUATED IN MAY 2024
BS in Electrical and Computer Engineering **Cumulative GPA**: 4.00

- **Awards and Honors:** Global Wildcat Award; Highest Academic Distinction and Dean's List 2020 – 2024

SKILLS

- **Software:** Microsoft Office, Google Drive, Visual Studio, Xilinx Vivado, Git, Ozone, Jira, J-Link
- **Technical:** Digital Circuit Design, Field-Programmable Gate Arrays (FPGA), Hardware Description Language, AVR, STM and EFR Microcontrollers, Circuit Analysis and Tools, Embedded Systems, Microwaves, Transmission Lines, GPUs, VLSI, HTML, CSS, Control Systems
- **Programming Languages:** C, C++, C#, CUDA, Verilog, MATLAB, Python
- **Language:** English, Spanish

PROJECTS

Autonomous Basketball Shooting Robot: Hoopster **Most Outstanding Project Award**

- Engineered an autonomous, mobile basketball shooting robot, "Hoopster," achieving a 95% free-throw accuracy
- Led the electrical, embedded, and computer vision aspects, ensuring seamless integration and functionality
- Developed embedded system code to control motors using PWM, and interfaced with sensors via UART, I2C, and interrupts for optimal performance
- Utilized yolov8 and OpenCV to train the system in identifying the basketball rim, enhancing shooting accuracy through advanced machine learning.
- Documented system requirements, testing procedures, risk analysis, and mitigation strategies during the project planning phase.

FPGA-based Pipelined Processor

- Complete understanding of processor design through FPGA based implementation of a custom pipelined Datapath and tradeoff analysis on the hardware-, software-, and instruction set architectures- design realms
- Designed and developed a five-stage general purpose pipelined processor with specialty in one task for a MIPS 32-bit ISA using a custom Variable Block Size Motion Estimator (VBSME) Assembly Code
- Conducted post implementation functional verification and implemented the design on the Xilinx Artix-7 FPGA
- Implemented a video compression algorithm in MIPS ISA and executed this program on the FPGA

PROFESSIONAL EXPERIENCE & LEADERSHIP EXPERIENCE

LUTRON ELECTRONICS *May 2023 – August 2023*
Embedded Software Engineering Intern

- Conducted in-depth research on STM and EFR microcontrollers, as well as their reference manuals, to gain a comprehensive understanding of the low layer register and interactions. This knowledge was crucial in implementing a new feature that utilized Direct Memory Access (DMA) and USART.
- Formulated a comprehensive list of customer requirements, along with system and software designs. These were essential in validating and describing the development and design of the feature, ensuring the realization of the necessary features.
- Employed C++ to fulfill the design and configure the required low-level registers for the DMA & USART modules.
- Utilized a J-Link device and Ozone for debugging to identifying and resolve issues to ensure optimal functionality.

Electrical and Computer Engineering *January 2022 – Current*
Teacher and Undergrad Lab Assistant (Computer Programming, Digital Logic, Computer Organization)

- Debugged students' C and Verilog codes, utilizing tools from Microsoft Visual Studio and Xilinx Vivado to ensure optimal functionality.
- Guided students through lab sessions and FPGA testing, vigilantly ensuring that safety protocols were adhered to at all times.
- Engaged in one-to-one interactions with students during lab sessions when required, fostering a deeper understanding of the course material.
- Stimulated students' problem-solving abilities and reinforced class material during lectures, promoting a comprehensive understanding of the subject matter